

AMENDMENTS TO THE CLAIMS

Please withdraw Claims 16-20 from consideration without prejudice. Please also add Claims 31 and 32.

Claims 1-15 (Previously cancelled)

Claims 16-20 (Cancelled)

21. (AMENDED) A method of fabricating a semiconductor device having a semiconductor region, the method comprising the steps of:

forming at least two conductive posts overlying the semiconductor region to form a structure;

encapsulating the structure and at least one of the at least two conductive posts to form a planarized cured passivation layer; and

exposing the at least one of the at least two conductive posts through the planarized cured passivation layer to form the semiconductor device, wherein the step of forming at least two conductive posts comprises a lift-off step.

22. (AMENDED) The method of Claim 21, wherein ~~the step of forming at least two conductive posts comprises a lift-off step, and~~ at least one of the at least ~~one~~ two conductive posts comprises at least one of Pt, Au and Ti.

23. (AMENDED) The method of Claim 21, wherein the step of encapsulating the structure and at least one of the at least two conductive posts comprises the steps of:

forming the passivation layer by spinning on benzocyclobutene ("BCB"); and

heating the passivation layer in an N₂ atmosphere to a temperature substantially in the range of 250-350°C for a period substantially in the range of 1-30 minutes, such that the passivation layer is spun on, cured and planarized.

24. (ORIGINAL) The method of Claim 21, wherein the step of exposing the at least one of the at least two conductive posts comprises the step of etching the planarized cured passivation layer.

25. (AMENDED) The method of Claim 24 32, wherein the ~~step of etching the planarized cured passivation layer comprises a~~ Reactive Ion Etching step and employs a chemistry of at least one of CF₄:O₂ at an approximate ratio of 40:60 and SF₆:O₂ at an approximate ratio of 6:10.

26. (AMENDED) A method of fabricating a semiconductor device having a semiconductor region, the method comprising the steps of:

forming at least two conductive posts of about the same height overlying the semiconductor region to form a structure;

encapsulating the structure and at least one of the at least two conductive posts to form a planarized cured passivation layer; and

exposing the at least one of the at least two conductive posts through the planarized cured passivation layer to form the semiconductor device, wherein the step of forming at least two conductive posts comprises a lift-off step.

27. (AMENDED) The method of Claim 26, wherein ~~the step of forming at least two conductive posts comprises a lift-off step, and~~ at least one of the at least two ~~one~~ conductive posts comprises at least one of Pt, Au and Ti.

28. (AMENDED) The method of Claim 26, wherein the step of encapsulating the structure and at least one of the at least two conductive posts comprises the steps of:

forming the passivation layer by spinning on benzocyclobutene ("BCB"); and

heating the passivation layer in an N₂ atmosphere to a temperature substantially in the range of 250-350°C for a period substantially in the range of 1-30 minutes, ~~such that~~ the passivation layer is spun on, cured and planarized.

29. (ORIGINAL) The method of Claim 26, wherein the step of exposing the at least one of the at least two conductive posts comprises the step of etching the planarized cured passivation layer.

30. (AMENDED) The method of Claim 29, wherein the step of etching the planarized cured passivation layer comprises a Reactive Ion Etching step ~~and employs a chemistry of at least one of CF₄:O₂ at an approximate ratio of 40:60 and SF₆:O₂ at an approximate ratio of 6:10.~~

31. (NEW) The method of Claim 30, wherein the ~~step of etching the planarized cured passivation layer comprises a~~ Reactive Ion Etching step and employs a chemistry of at least one of CF₄:O₂ at an approximate ratio of 40:60 and SF₆:O₂ at an approximate ratio of 6:10.

32. (NEW) The method of Claim 24, wherein the step of etching the planarized cured passivation layer comprises a Reactive Ion Etching step.